Abstract

The invention concerns semiconductor latches capable of memorizing any programmed information even after power supply has been removed. Used is a 0.6 m BiCMOS EPROM process but it is applicable in any other process having hot electron injection devices like EPROM, Flash EEPROM. Suggested is a bi-stable latch circuit having a pair of cross-coupled branches (I,II), each branch including a complementary driver and a load connected between a drain line and a source line and a non-volatile memory cell having a program transistor and a read transistor, at least one of said drivers and loads including said read transistor, said driver and load of said branch connected in series at a respective output node, said read transistor and program transistor having a common floating gate and separate control gates, said control gate of said program transistor connected to a program voltage, the drain of said program transistor connected to a respective input node, said control gate of said read transistor in said branch connected to said output node of the other branch (II).